

REMARKS

A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Claims 31, 34 and 40 are currently amended.

Claims 1-20, 33 and 37 are now canceled.

No new matter has been added.

Allowable Subject Matter

Applicants appreciate the allowance of claims 21-30.

The Examiner has also indicated that claims 33, 34 and 40 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, applicants have amended base claim 31 by adding the limitations of now canceled claim 33 thereto, and have amended the dependency of claim 34. Applicants have also included the limitations of base claim 31 into now independent claim 40. In view of the foregoing, it is submitted that claims 31, 32 and 34-40 are now in a condition for allowance.

The Examiner has also requested the non-patent literature/other art that was filed as part of the IDS of 11/25/2003. Accordingly, applicants are submitting herewith copies of such non-patent literature as identified below:

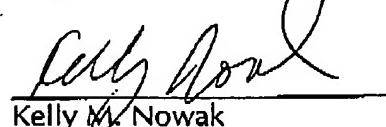
"A Novel Trench DRAM Cell with a VERTical Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.

"Extending Trench DRAM Technology to 0.15 μ m Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.

"A 0.135 μ m² 6F² Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 80-81, IEEE, 2000.

In view of the foregoing, applicants respectfully submit that the application is in a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



Kelly M. Nowak
Reg. No. 47,898

DeLIO & PETERSON, LLC
121 Whitney Avenue
New Haven, CT 06510-1241
(203) 787-0595

A Novel Trench DRAM Cell with a VERtical Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb

U. Gruening, C.J. Radens^{*}, J.A. Mandelman^{*}, A. Michaelis, M. Seitz, N. Arnold, D. Lea^{*}, D. Casarotto, A. Knorr, S. Halle^{*}, T.H. Ivers^{*}, L. Economikos^{*}, S. Kudelka, S. Rahn, H. Tews, H. Lee, R. Divakaruni, J.J. Welser^{*}, T. Furukawa^{**}, T.S. Kanarsky^{*}, J. Alsmeyer, G.B. Bronner

^{*}Infineon Technologies, Corp., Hopewell Junction, NY 12533, USA
^{*}IBM Semiconductor R&D Center, Hopewell Junction, NY 12533, USA
^{*}IBM T.J. Watson Research Center, Yorktown Heights, NY
^{**}IBM Microelectronics, Essex Junction, VT

Abstract

Results are presented for a novel trench capacitor DRAM cell using a vertical access transistor along the storage trench sidewall which effectively decouples the gate length from the lithographic groundrule. A unique feature of this cell is the vertical access transistor in the array which is self-aligned to the buried strap [1] connection of the storage trench (VERI BEST) and bounded by trench isolation oxide. The VERI BEST cell concept, process and electrical results obtained from 8F² test cell arrays at 0.175μm groundrules are described in this paper.

Introduction

With each new generation the available space for the channel length of the DRAM transfer device continues to shrink aggressively. Conventional scaling techniques are limited by

the stringent leakage requirements of a DRAM cell as shown in Fig. 1: A reduction in gate poly length requires thinner gate oxides and increased channel doping to avoid short channel effects. High doping levels, however, lead to increased junction leakage which decreases data retention time [2]. At the same time gate oxide reliability requires reduction of the wordline voltage, thus degrading the charge writeback characteristics and signal margin, as the array threshold voltage remains fixed due to off-current requirements. Therefore a vertical array transistor is proposed as a means to decouple the gate length from the shrink path.

The proposed VERI BEST process is based on the advanced BEST [3] cell technology with a planar array transistor and raised shallow trench isolation [4] and a vertical pass transistor along the deep trench sidewall [5]. Cross-sectional views in Fig. 2 show the evolution from a conventional 8F² planar MOSFET cell to the VERI BEST cell, as well as a

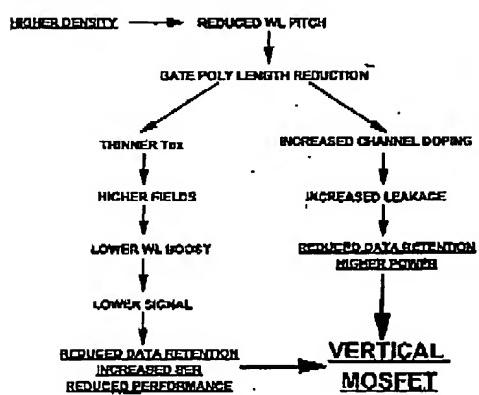


Fig. 1: Motivation for vertical access MOSFET for DRAM scalability.

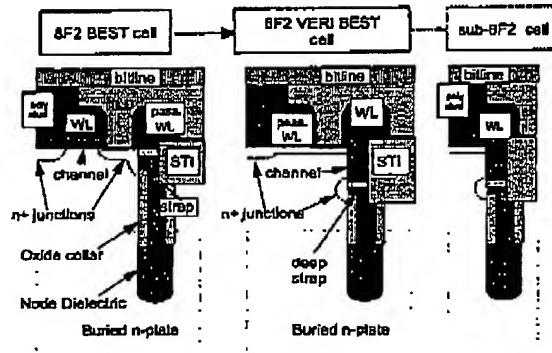


Fig. 2: Evolution from a planar 8F² to vertical MOSFET cells:
(a) State-of-the-art 8F² DRAM with planar channel, (b) Novel 8F² DRAM cell with a vertical transistor channel on top of the deep trench storage capacitor (c) Potential shrink path to sub-8F² cells.

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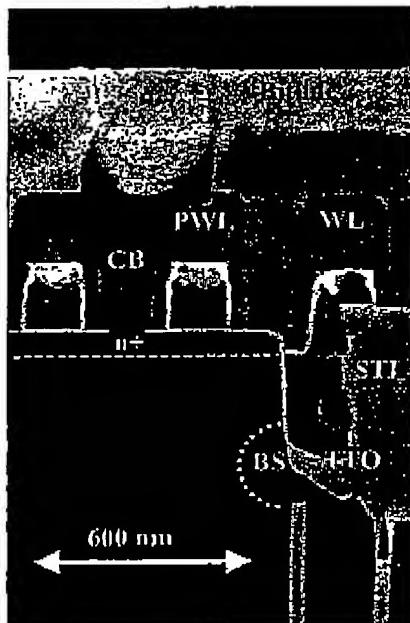


Fig. 3: SEM picture of 8F² VERTI BEST cell with vertical transistor, showing same X-sectional view as sketched in Fig. 2

potential shrink path to sub-8F² cells. From an addressing point of view, the two 8F² cells are transformed into each other by exchanging logically the role of the active and passing wordlines (WL). The vertical transistor is now controlled by the formerly passing WL running across the top of the deep trench, its channel length being determined by the depth of a recess etch which can be optimized independently of the groundrule. Fig. 3 shows a SEM picture of the fabricated structure.

Process Flow

Fig. 4 shows schematically the process flow, as summarized in Table I. After forming the deep storage trench capacitor, the poly recess etch determining the buried strap depth is extended by about 0.3-0.4 μm in order to accommodate space for the vertical transistor, followed by collar oxide removal and buried strap formation (Fig. 4a). The buried strap polysilicon is then covered with a trench top oxide (TTO) layer to insulate the node from the vertical gate poly and the pad layers are stripped. After implanting the wells for the array and support devices and the array n⁺-bitline junction, a gate oxide is grown (Fig. 4b) both at the planar surface and

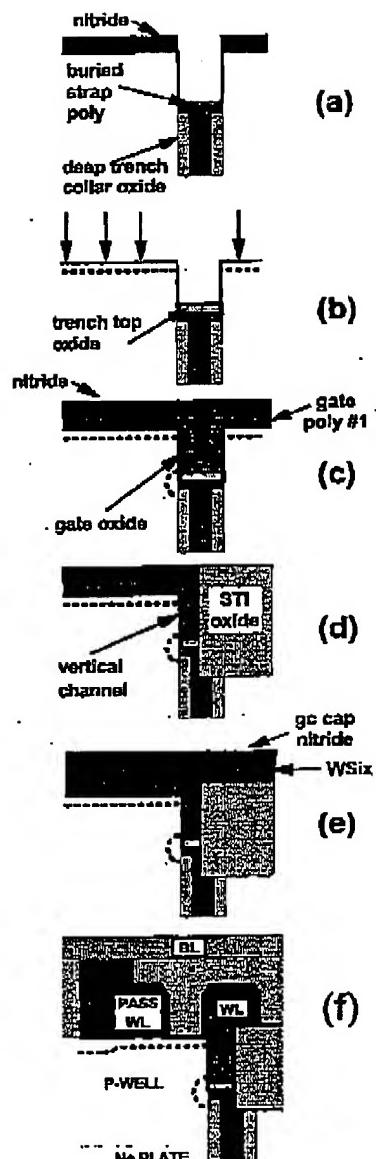


Fig.4: Key process steps for the formation of the vertical MOSFET.

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TABLE I
Summary for key process steps corresponding to Fig. 4

(a)	STORAGE TRENCH and BURIED-STRAP CONNECTION
(b)	TRENCH TOP OXIDE ISOLATION and WELL and N ⁺ ARRAY JCT IMPLANTS
(c)	GATE OXIDATION and GATE POLY #1 DEPOSITION
(d)	SHALLOW TRENCH ISOLATION
(e)	GATE POLY/WSi _x DEPOSITION
•	ETCH GATES and IMPLANT JCTS
▪	INTERLEVEL DIELECTRIC
(f)	CONTACTS and BITLINE FORMATION

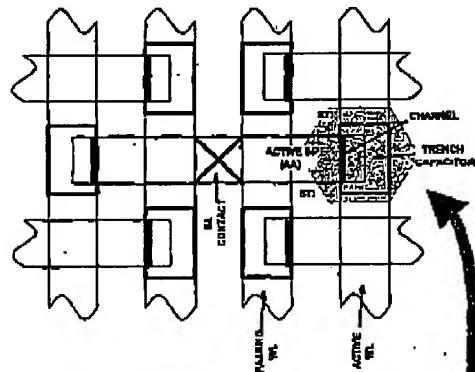


Fig. 5: Layout of the BP³ array containing vertical MOSFET

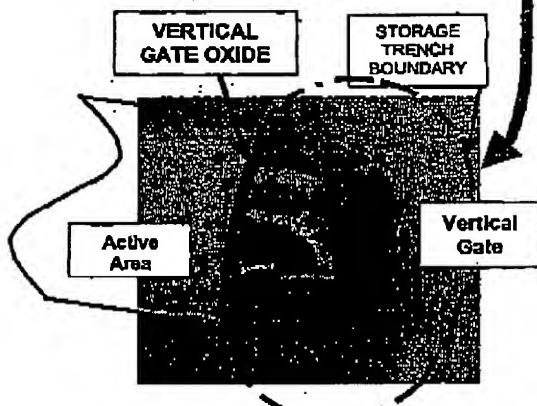


Fig. 6: TEM plan view (from shaded inset in Fig. 5, cut through vertical gate) showing gate oxide formed on <110> crystallographic sidewall of active silicon area (AA).

along the exposed portions of the trench sidewall, and covered with a first gate polysilicon layer (Fig. 4c). Then isolation trenches are etched to a depth below the buried strap and filled with oxide, ensuring the isolation of the storage trenches and defining the edges of the vertical device (Fig. 4d and layout in Fig. 5). After depositing a poly/WSi_x/SiN layer (Fig. 4e) onto the first gate polysilicon layer, the gate conductors are patterned and etched simultaneously in the array and planar support device regions. Then conventional source/drain and self-aligned contact processing is used to complete the structure as shown in Fig. 4f.

Experimental Results

As shown by the layout in Fig. 5, the isolation trench defines the boundary for the vertical array device. The vertical channel is formed only along the <110>-crystallographic orientation portion of the storage trench sidewall which remains after the isolation trench etch. Fig. 6 shows a plan view TEM of a vertical gate oxide with 9 nm thickness as well as the vertical part of the gate polysilicon. A heavy shallow arsenic implant is performed prior to the gate oxidation to form the bitline diffusion, providing a conductive path under the passing wordline as sketched in Fig. 2. The array V_t is controlled by a boron peak centered in the channel (Fig. 7), which allows minimization of the well doping at the node junction, for a low defect-induced leakage.

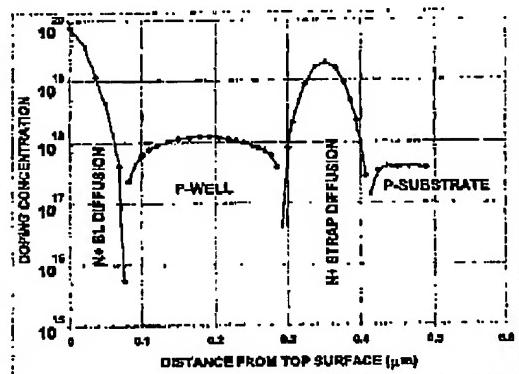


Fig. 7: Simulated vertical doping profile along gated sidewall of storage trench.

The effective channel length is typically 0.2 μm, dependent on the chosen recess depth. Due to the longer channel length, the device can be operated on the flat part of the roll-off curve, allowing a good threshold voltage control. Fig. 8 shows a cross-section SEM of 0.54 μm deep isolation trenches after oxide fill and CMP oxide planarization. A void free trench fill with an aspect ratio of more than 4 has been achieved by

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using an advanced high density plasma (HDP) oxide gap fill process.

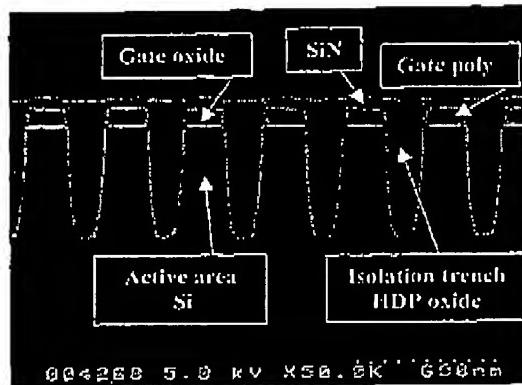


Fig. 8: SEM showing voidless filling of high aspect ratio isolation trenches after oxide planarization

Measured values of sub-threshold slope are approximately 100mV/dec at 85°C (Fig. 9), yielding an extrapolated off-current which is significantly less than the I_{off}/device required for long retention time.

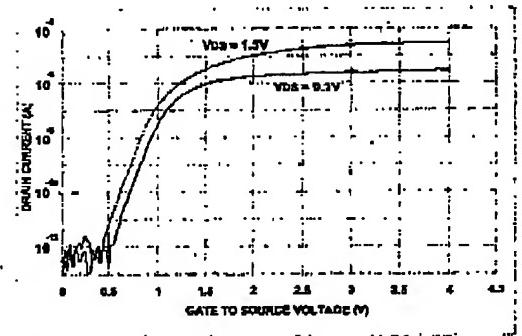


Fig. 9: Measured I_D - V_G characteristics demonstrating low off-current

A test chip with 1Mbit (4x256kbit) VERI BEST cell arrays at a design rule of 0.175μm was fabricated and tested with standard parameters. The test results of such an array indicate similar yield behavior as planar array device technology in the same stage of development. Fig. 10 shows a bitfail map of a 1Mbit array at 2ms screen test, demonstrating the cell

functionality. The median retention time is measured to be greater than 5 sec at 85°C, confirming the good leakage properties obtainable with a vertical array device.

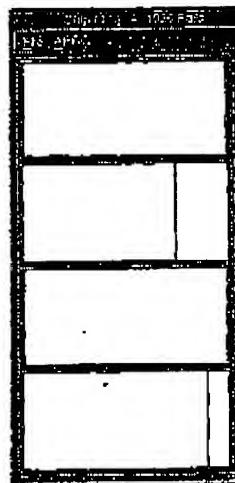


Fig. 10: Bitfail map of 1Mbit array, demonstrating cell functionality.

Conclusions

In summary, we have demonstrated the integration and functionality of a novel DRAM trench cell using a vertical access transistor that is suitable for the next Gb-DRAM generations. It has been shown that the vertical array transistor is able to meet DRAM retention time requirements, thus enabling future cell scaling independent of transistor channel length.

Acknowledgements

The authors would like to thank all project contributors from the DRAM Development Alliance of IBM and Infineon and the IBM ASTC facility for their continuous support.

References

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9.1 A $0.135 \mu\text{m}^2$ 6F² Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM

C. J. Radens⁺, U. Gruening⁺, J. A. Mandelman⁺, M. Seitz⁺, T. Dycr⁺, D. Lea⁺, D. Casarotto⁺, L. Clevenger⁺, L. Nesbit⁺, R. Malik⁺, S. Halle⁺, S. Kudelka⁺, H. Tews⁺, R. Divakaruni⁺, J. Sim⁺, A. Strong⁺, D. Tibbel⁺, N. Arnold⁺, S. Bukofsky⁺, J. Preuninger⁺, G. Kunkel⁺, G. Bronner⁺

⁺ IBM Microelectronics, Semiconductor R&D Center, 1580 Route 52, Hopewell Junction, NY 12533

⁺ Infineon Technologies, 1580 Route 52, Hopewell Junction, NY 12533

DRAM Development Alliance IBM / Infineon
IBM Semiconductor Research & Development Center, 1580 Route 52, Hopewell Junction, NY 12533

Abstract

A $0.135 \mu\text{m}^2$ trench-capacitor DRAM cell with a trench-sidewall vertical-channel array device has been fabricated using 150 nm groundrules and optical lithography. This 6F² cell features a novel active area layout, a trench-top-oxide (TTO) isolation between trench capacitor and trench gate, maskless self-aligned buried strap node contact, shallow trench isolation (STI), a self-aligned poly-plug bit contact, and two levels of bitline interconnect, both formed using a W dual-damascene process.

Introduction

The continued characteristic shrinking of DRAM technology will require the development of a compact and scalable DRAM array cell in addition to improvements in lithographic patterning. As the array cell layout is compressed, the bit contact and node diffusions encroach upon the device channel region, V_t control is reduced, and variation is introduced in I_{DS} and data retention; it is desired to decouple the array transistor channel length from the lithographic groundrule critical dimension. Vertical transistors have been proposed to address these problems [1,2,3]. In addition, a sub-8F² DRAM will require an alternative to the folded bitline architecture [3,4]. This paper describes a scalable 6F² trench-capacitor-sidewall vertical transistor cell with a herringbone active area layout and two levels of bitline wiring.

Cell Structure and Design Concept

The 6F² array cell layout is shown in Fig. 1. The herringbone active area pattern affords the maximum separation between each pair of devices while maintaining a 2F minimum-pitch wordline. Fig 2 shows the cell cross section including the upper region of the trench capacitor device. The device channel and maskless buried strap node contact is formed at the intersection of the trench and active area pattern. The channel V_t and array well doping profile is adjusted to set the maximum dopant concentration localized away from the buried strap node outdiffusion. Within the constraints of buried strap outdiffusion shown in Fig 3, further compaction of the cell area may be obtained by a reduction of the 3F bitline pitch. Two levels of bitline wiring are interchanged at intervals over the array to provide folded sensing on the scale of the bitline interchange interval [4,5].

Fabrication

A fully-planarized process sequence with a VERT-BEST [3] raised-shallow-trench isolation [6] is used to concurrently form the vertical array and planar support devices. The capacitor is formed using a LOCOS collar [7]. Anisotropic

deposition of the trench-top oxide (TTO) isolates the upper-trench gate polysilicon from the lower-trench storage node, and is also used for the STI. The self-aligned buried strap is formed by the outdiffusion of As from the capacitor polysilicon. The vertical device and planar support gate oxide and gate poly are formed prior to the delineation of the STI. Critical levels are patterned using a 248 nm system with 0.68 N.A., and attenuated phase-shift masks. A summary of the process flow is shown in Fig 4.

Results

An SEM top-down view of the deep trench (DT) and herringbone active area (AA) pattern with STI oxide removed is shown in Fig 5. The DT lithography shows a sensitivity to focus and lens aberrations. An SEM cross-section view of a pair of the completed cells along the <100> plane of the active area is shown in Fig 6. The buried strap outdiffusion is approximately 50 nm. A channel length of ~200 nm is obtained with the 150 nm groundrule process technology. The channel is formed along a corner of the trench RTO gate oxidation with a rate ratio for <100>/<110> of 0.9 is shown in Fig 7. The reliability of the RTO gate dielectric along <110> with $\beta > 2$ and projected lifetime >10 years is shown in Fig 8. The array transistor characteristics, measured through a pair of back-to-back transistors in series, is shown in Fig 9 and Fig 10. Due to the series resistance of the pass transistor, the measured drive current does not directly indicate the single transistor performance. Screen bit fail maps from a 1Mb array diagnostic monitor test chip with a) perfect 7F² array and b) low-density of failures in the 6F² array are shown in Fig 11. A summary table including selected parametric attributes is shown in Fig 12.

Conclusions

A functional $0.135 \mu\text{m}^2$ 6F² DRAM cell has been demonstrated using a trench-sidewall vertical access transistor at a 150 nm groundrule. Optimization of a reliable and orientation-independent gate oxidation, and shallow strap outdiffusion is required to maintain device performance. This cell and the dual bitline architecture shows the potential for continued extension of trench DRAM technology.

References

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- [5] H. Hoeningschmid, Symp. VLSI Circ., p36, 1998
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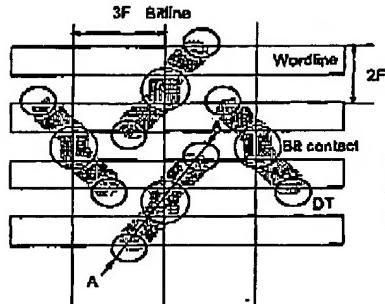
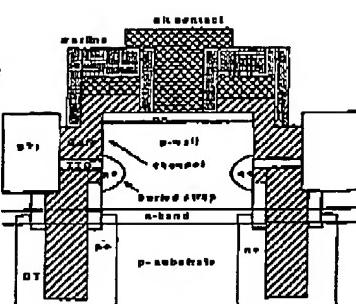
Fig 1. 6F² vertical cell layout

Fig 2. Schematic cross section along AA showing a pair of devices.

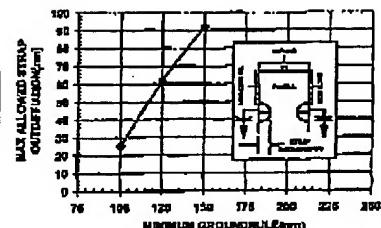


Fig 3. Maximum allowed strap outdiffusion to prevent device-to-device interaction

1. Trench capacitor
2. Buried plate and LOCOS collar
3. Maskless buried strap contact
4. Trench top isolation (TTI)
5. Device and well I/I
6. Gate oxidation and poly deposition
7. Shallow Trench Isolation (STI)
8. Planar support gate and wordline pattern
9. Source/drain I/I and activation
10. Contacts and interconnect

Fig 4. Process flow summary

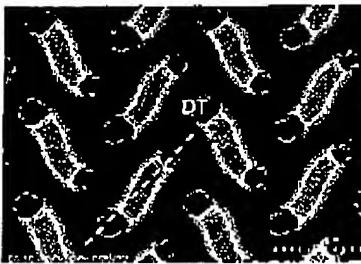


Fig 5. Top-down SEM of trench (DT) and active area (AA) with STI removed.

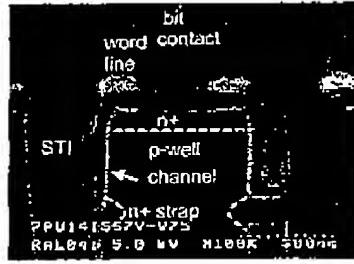


Fig 6. Cross section SEM along AA.

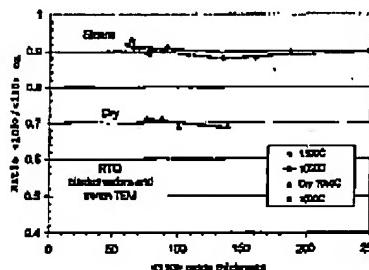
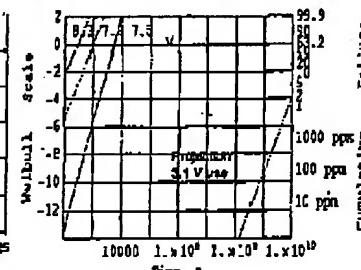
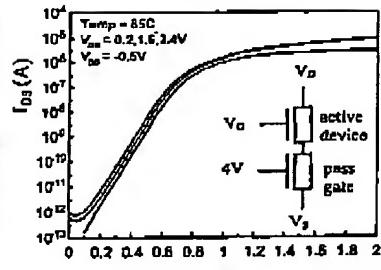
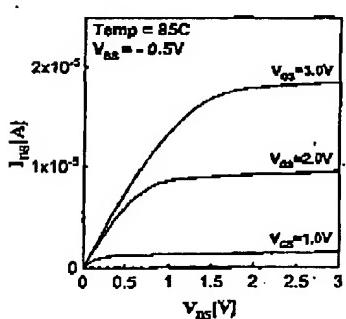
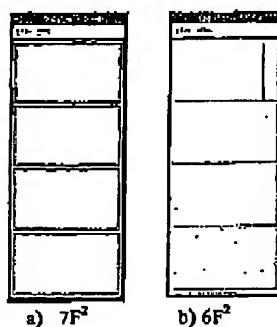


Fig 7. Orientation-dependant oxidation.

Fig 8. Reliability of <110> 6.8 nm oxide, 0.1 mm², 140 C, $\beta = 2.4$, $\gamma = 3.66$ Fig 9. I_D vs. V_G and V_{DS} measured through back-to-back active and pass devicesFig 10. I_G vs. V_D and V_G measured through back-to-back devicesFig 11. 1Mb array screen bit fail map
a) perfect 7F², b) low-fail density 6F²

Cell area = 0.135 μm^2
Min. pitch = 300 nm
Groundrule = 150 nm
Deep trench storage capacitor
Node = 3.8 nm
Cnode = 25 fF/cell
Tox array = 6.8 nm
Median retention = 2 sec
Polysilicon stud bit contact stud
Rc bit contact < 3 k Ω /contact
Rc strap node contact < 15 k Ω /bit
2 levels W and 2 levels Al interconnect

Fig 12. Cell summary

Extending Trench DRAM Technology to 0.15 μ m Groundrule and Beyond

T.Rupp#, N.Chaudhary#, K.Dev#, Y.Fukuzaki♦, J.Gambino*, H.Ho*, J.Iba♦, E.Ito♦, E.Kiewra*, B.Kim*, M.Maldei#, T.Matsunaga♦, J.Ning#, R.Rengarajan#, A.Sudo♦, Y.Takegawa♦, D.Többen#, M.Weybright*, G.K.Worth*, R.Divakaruni*, R.Srinivasan*, J.Alsmeier#, G.Bronner*

*IBM, #Infineon Technologies, ♦Toshiba at DRAM Development Alliance, IBM Semiconductor R&D Center, 1580 Route 52, Zip33A, Hopewell Junction, NY 12533, USA

Abstract

This report describes improvements in the trench DRAM technology for 0.15 μ m groundrule and beyond. The optimum cell layout is 8F² with a cell area of only 0.18 μ m² for a 0.15 μ m groundrule. High node capacitance and low node contact resistance are demonstrated for these small groundrules. By using a dual gate oxide and self-aligned support junctions, the different performance requirements of array and support devices can be met. These technology features and their extendibility are evaluated on a 256Mb DRAM design.

Introduction

The self-aligned buried strap (BEST) trench DRAM cell [1][2] can be scaled for future DRAM generations. Trench capacitors provide a more planar surface than stacked capacitors [2], resulting in a larger process window for lithography and etch. A conventional folded bitline architecture with an 8F² layout has many design advantages and can be used for several shrink generations (Fig. 1).

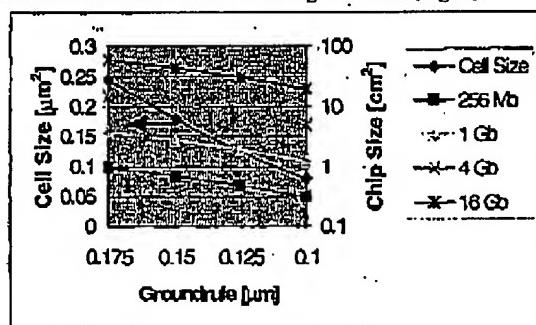


Fig. 1. DRAM cell size of 8F² layout for different ground-rules. Resulting chip sizes for various DRAM generations are shown (65% array efficiency).

Further cell size reduction below 8F² is possible [3] but results in an open bitline architecture, requires two levels of bitline wiring and has device scaling problems. The 8F² cell (Fig. 2) is good for lithography due to its very symmetrical layout, an equal line space pattern, and optimal overlay tolerances. The inherent challenge for reducing feature size is in maintaining basic DRAM parameters such as cell capacitance, resistances, device leakage and performance while shrinking the dimensions. This work focuses on extending these parameters for future DRAM generations.

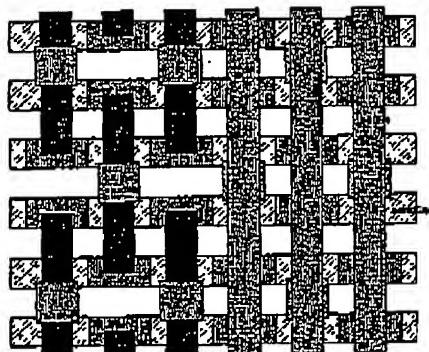


Fig. 2. 8F² layout. The wordlines and bitlines are at minimum pitch; bidines are shown only on the right half of the layout. The deep trench (DT) size is nominally 2F. The bitline contacts are borderless and self-aligned to gates and shallow trench isolation (STI). The buried strap is formed by the overlap of active area and trench capacitor.

Process and Results

The process starts with etching of the deep trenches into a p-substrate. For the locally oxidized (LOCOS) collar process [4] a SiN barrier layer is deposited, the trenches are filled with resist and the resist is recessed to the bottom of the collar (Fig. 3a). The SiN barrier is etched in the upper part of the trench, opening the silicon (Si) for subsequent LOCOS oxidation (Fig. 3b). The thermal SiO₂ thickness is 37 nm. Using isotropic Si etching, the bottom part of the trench can be enlarged to form a bottle [4] (Fig. 3c). Thereafter, the buried n-plate can be formed self-aligned to the collar using gas phase or plasma doping (Fig. 3d). Fig. 4 shows the capacitor trenches after poly deposition in the small (Fig. 4a) and long directions (Fig. 4b) of the trench.

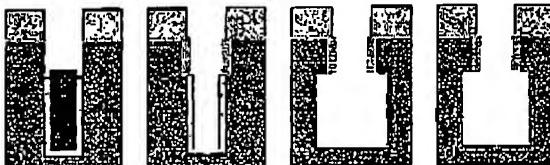


Fig. 3. LOCOS collar process. bottle capacitor enhancement and self-aligned buried plate. a) Resist recess for SiN barrier definition. b) LOCOS oxidation after barrier etch and resist strip. c) Bottle enlargement using isotropic Si etching. d) Buried plate formation self-aligned to the collar.

Widening the deep trench by 40 nm per edge increases the calculated capacitance by more than 40% (Fig. 5). The

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measured capacitance for a 5 μm deep trench increases from 22 fF to 33 fF for this 40 nm bottle widening.

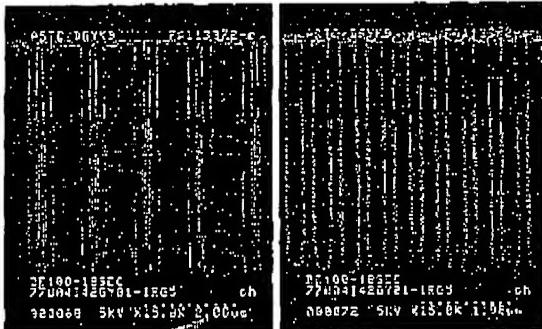


Fig. 4. Trench capacitor after recess to define the buried strap (BS) bottom.
a) Cross-section perpendicular to the wordline (short side of the trench).
b) Cross-section parallel to the wordline (long side of the trench).

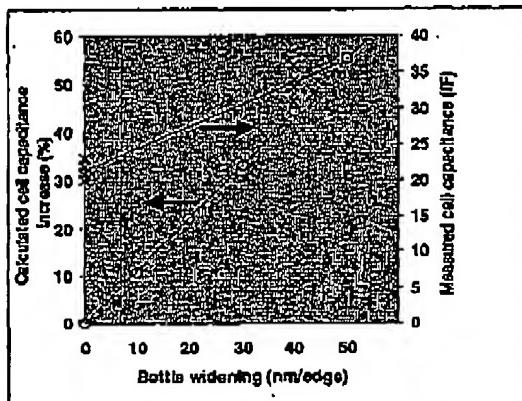


Fig. 5. Cell capacitance increase versus DT bottle widening. A widening of 40 nm results in a calculated capacitance increase of 40%. For a 5 μm deep trench the measured capacitance changes from 22 fF up to 33 fF.

A conventional Buried Strap (BS) connection (Fig. 6a) is defined by the overlap between active area and deep trench. The not covered part of the trench, filled with poly Si, is removed during the shallow trench isolation (STI) process. Therefore the connection and the resistance between the trench and the active area is depending on the overlay (Fig. 7a). A self-aligned oxide hard mask STI process (Fig. 6b) is applied to eliminate the overlap dependence as well as to increase the size of the connection region (Fig. 7b). Key processes are nitride RIE selective to oxide during mask open and Si RIE selective to oxide (hard mask material). The total resistance defined as the sum of interface and poly strap is reduced by more than half from 11 down to 4.5 k Ω with this self-aligned process (Fig. 8), implying further scalability as well as improved device performance in the current generation. To further improve the array device performance a reduction of the height of the BS opening is critical and

affords a controlled recess to reduce the overlap to the active wordline.

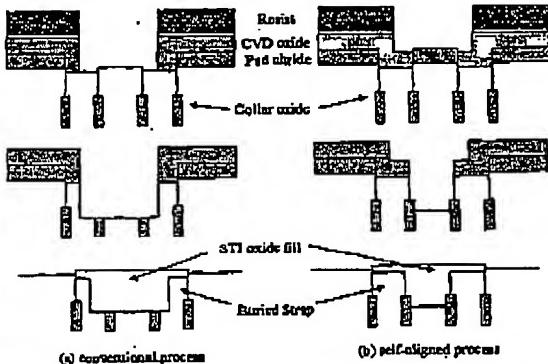


Fig. 6. Conventional (a) and self-aligned (b) STI process sequence.

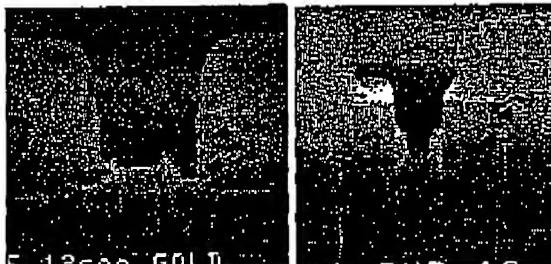


Fig. 7. SEMs of buried strap (BS) connection perpendicular to the WL.
a) Conventional STI process; overlay sensitive. b) Self-aligned hard mask process; buried strap connection using the complete DT width.

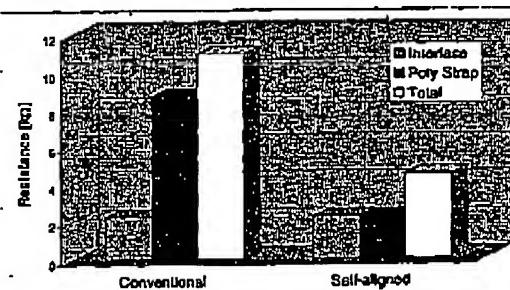
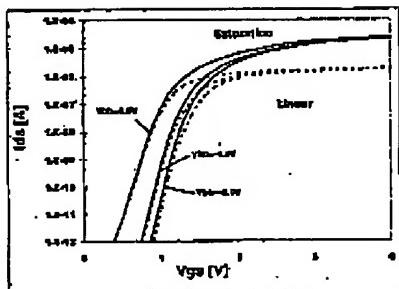


Fig. 8. Comparison of BS resistance with different connection methods.

The transistors are formed in retrograde n- and p-wells. The n-well is also used to connect the buried plate. A 35 / 55A dual gate oxide process using nitrogen implantation [5] is implemented, in order to improve the performance of the DRAM peripheral devices independent of the array.

Fig. 9 shows a typical Vg-Id curve for the array device. The subthreshold slope of 95 mV/dec for this W/L=0.150/0.150 μm device results in an off-current adequate for the array device.

2.3.2

Fig. 9. Typical V_g - I_d curve for the array device ($W/L=0.150/0.150 \mu\text{m}$).

The use of a single n-type poly Si gate results in the p-FET's being of the buried channel type. Indium and antimony retrograde channel implants (n-well see Fig. 10), thin gate oxide, halo implantation and a reduced thermal budget are used to improve the support device roll-off. Roll-off curves for nominal and low V_t n-FET and p-FET are shown in Fig. 11 and Fig. 12. Unlike surface channel devices, the V_t of a buried channel device, decreases with increasing gate oxide thickness [6]. This characteristic is taken advantage of using a thick gate oxide for the low V_t p-FET. The increase in subthreshold slope with decreasing gate length is one of the main challenges in buried channel p-FET scaling [6] but can be overcome with the implemented improvements (Fig. 13). The wordlines are composed of an n-type poly Si/WSi gate stack and are completely encapsulated with SiN to provide isolation for the self-aligned array contact [7].

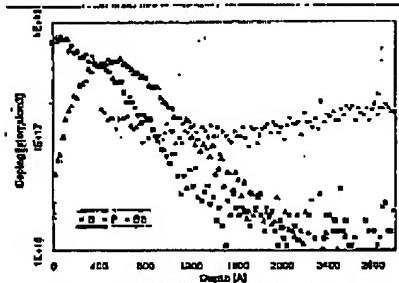
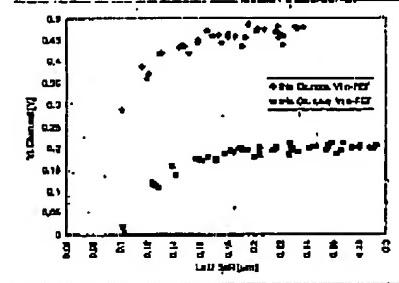
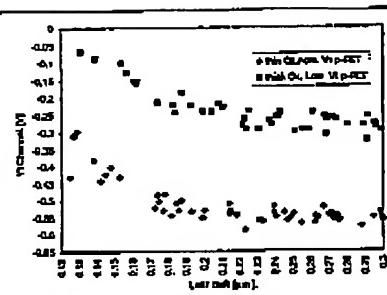
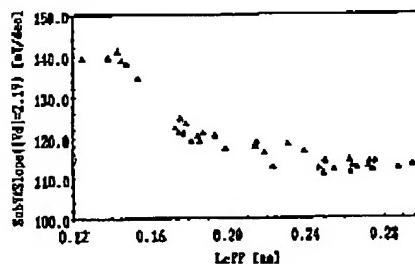


Fig. 10. Final SIMS profile of the retrograde n-well implant.

Fig. 11. Roll-off curve for thin oxide nominal and low V_t n-FET.Fig. 12. Roll-off curve for a thin oxide nominal V_t and a thick oxide low V_t buried channel p-FET.Fig. 13. Subthreshold slope for nominal V_t thin oxide p-FET.

The contact implant uses a self-aligned spacer implant scheme with a disposable oxide spacer (Fig. 14b). Compared to a conventional contact implant (Fig. 14a), this scheme is self-aligned to the gates and has advantages in the overlay sensitivity of the contact level as well as a relaxed groundrule for the alignment to the gates.

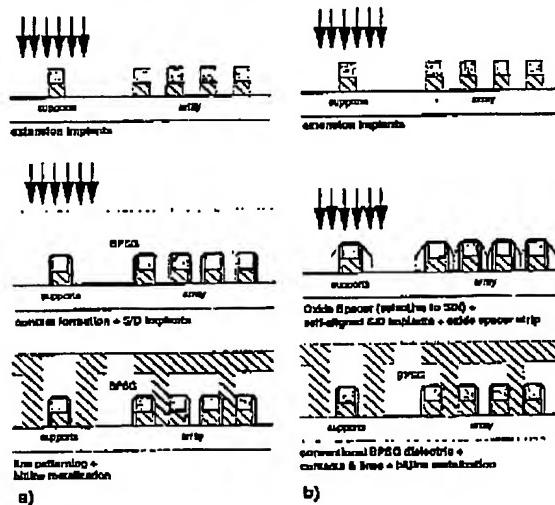


Fig. 14. Different S/D implant schemes are shown above. a) Implant through the contact opening. b) Self-aligned spacer implant.

2.3.3

Due to the high dose implant in the complete junction area the area capacitance is reduced to $1.32 \text{ fF}/\mu\text{m}^2$ (n-FET) and $1.24 \text{ fF}/\mu\text{m}^2$ (p-FET) compared to the contact implant scheme $2.15 \text{ fF}/\mu\text{m}^2$ (n- and p-FET). After S/D implantation the oxide spacers (Fig. 15a) formed in the supports and also filling the array spaces (Fig. 15b) are stripped selectively to the SiN liner using HF chemistry.

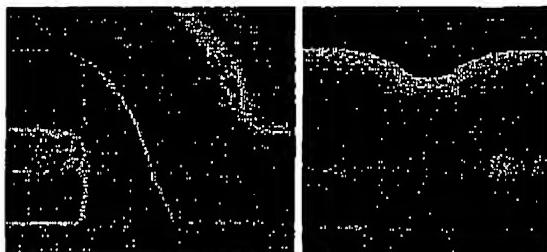


Fig. 15. SEM cross-sections after oxide spacer formation. a) Support region with 90nm oxide spacer. b) Array region filled with remaining void, making the disposing of the oxide spacer necessary.

BPSG deposition and reflow is used for void-free filling of the array, followed by a CMP planarization, stopping on top of the gates [8]. The self-aligned bitline contact is etched and filled with poly Si, forming a poly Si stud. Contacts to gates and diffusions in the supports are formed simultaneously, using a tungsten (W) dual damascene process. A cross-section of the array up to the bitline metal level is shown in Fig. 16.

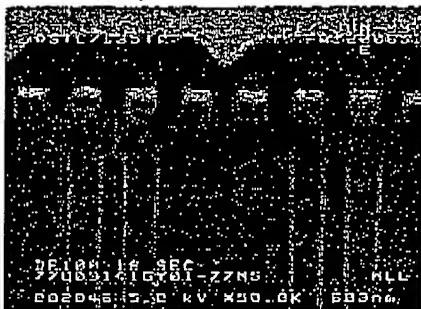


Fig. 16. SEM cross-section of DRAM array perpendicular to the wordlines up to the first metal level showing LOCOS collar and self-aligned STI.

The next metal level after the bidines uses W damascene vias. Due to the full planarization scheme available in the trench DRAM technology there is no topography between array and support region. The first aluminum (Al) metal level can therefore be wired on a groundrule pitch to support a wordline stitch architecture resulting in a faster signal processing. A sandwich layer (bottom up) of Ti/TiN/Al-Cu/Ti/TiN is deposited and etched using Al reactive ion etching (RIE) [9]. The undoped SiO₂ passivation results in a void-free fill for a $0.15 \mu\text{m}$ groundrule (Fig. 17). The second Al metal level is on a relaxed pitch, a tapered via below allows for Al via fill and metal deposition with one process

step. This second Al metal is also patterned by RIE and a final passivation is performed to protect the structure.

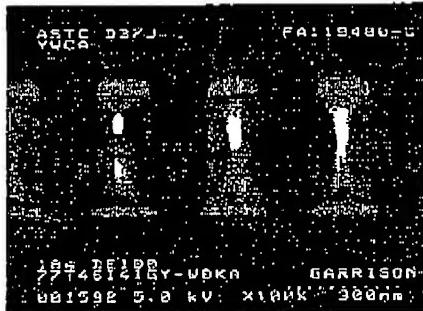


Fig. 17. First Al metal wiring on $0.15 \mu\text{m}$ pitch over the array. The stack is a sandwich layer of Ti/TiN/Al-Cu/Ti/TiN. The SiO₂ fill is void-free.

Conclusion

We have demonstrated an 8F² DRAM cell for $0.15 \mu\text{m}$ groundrule. To overcome the challenges of shrinking dimensions we introduced several self-aligned features. Dual gate oxide devices, retrograde wells, halo implantation and low thermal budget result in high performance devices. An Al metal etch is used for on pitch wordline stitching. The discussed features guarantee a high yielding and manufacturable process and provide potential for future shrink generations.

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2.3.4